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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/630,516	07/29/2003	David W. Hansquine	030192	7900
7590	05/02/2005		EXAMINER	
QUALCOMM Incorporated Attn: Patent Department 5775 Morehouse Drive San Diego, CA 92121-1714			BARAN, MARY C	
			ART UNIT	PAPER NUMBER
			2857	

DATE MAILED: 05/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/630,516	HANSQUINE ET AL. 	
	Examiner Mary Kate B. Baran	Art Unit 2857	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) Responsive to communication(s) filed on 02 December 2004.
- 2a) This action is FINAL.                    2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) Claim(s) 1-31 is/are pending in the application.
  - 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) Claim(s) \_\_\_\_\_ is/are allowed.
- 6) Claim(s) 1-31 is/are rejected.
- 7) Claim(s) \_\_\_\_\_ is/are objected to.
- 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on 29 July 2003 is/are: a) accepted or b) objected to by the Examiner.
 

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
  - a) All    b) Some \* c) None of:
    1. Certified copies of the priority documents have been received.
    2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
    3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |   |   |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)                     |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)  | Paper No(s)/Mail Date. _____.   |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date <u>02 December 2004</u> . | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
|   | 6) <input type="checkbox"/> Other: _____.                                   |

## DETAILED ACTION

### ***Specification***

1. The disclosure is objected to because of the following informalities:
  - (a) On page 3 [0010] line 7, "not distributed" should be – not be distributed –.
  - (b) On page 16 [0072] line 2, "includes and" should be – include an –.
  - (c) On page 16 [0073] line 2, "includes" should be – include –.
  - (d) On page 17 [0075] line 4, "issues" should be – issue –.
  - (e) On page 18 [0079] line 4, "compares" should be – compare –.

Appropriate correction is required.

### ***Claim Objections***

2. Claims 2, 8, 10, 16, 19, 24 and 26 are objected to because of the following informalities:
    - (a) Claim 2 page 20 line 2, "one of set" should be – one of a set –.
    - (b) Claim 8 page 21 line 3, "commands" should be – commands. –.
    - (c) Claim 10 page 21 line 3, "between least" should be – between at least –.
    - (d) Claim 16 page 22 line 3, "applied based an" should be – based on an –.
    - (e) Claim 19 page 23 line 2, "define" should be – defines –.
    - (f) Claim 24 page 23 line 2, "coupled the" should be – coupled to the –.
    - (g) Claim 26 page 24 line 5, "issue" should be – issuing –.
- Appropriate correction is required.

***Claim Rejections - 35 USC § 102***

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-6, 19, 22, 23 and 25-29 are rejected under 35 U.S.C. 102(b) as being anticipated by Crouch et al. (U.S. Patent No. 5,995,731) (hereinafter Crouch).

Referring to claim 1, Crouch teaches a system comprising a built-in self-test (BIST) controller that stores a set of commands defining an algorithm for testing a memory module (see Crouch, Figure 2 “BIST Controller 210”); a sequencer that receives the commands and issues one or more memory operations in accordance with the commands (see Crouch, column 2 lines 6-9); and a memory interface that applies the memory operations to the memory module in accordance with physical characteristics of the memory module (see Crouch, Figure 2 “Memory 215”).

Referring to claim 2, Crouch teaches an algorithm memory that stores the set of commands as one of a set of selectable memory test algorithms having associated commands (see Crouch, column 6 lines 10-18); and an algorithm controller to retrieve the commands from the algorithm memory and issue the commands associated with the selected memory test algorithm to the sequencer (see Crouch, column 6 lines 18-22).

Referring to claim 3, Crouch teaches an interface to receive one or more additional memory test algorithms, wherein the algorithm controller delivers the additional memory test algorithm to the sequencer for application to the memory interface (see Crouch, column 8 lines 16-28).

Referring to claim 4, Crouch teaches that the memory interface comprises one or a plurality of memory interfaces associated with respective memory modules, and the sequencer comprises one of a plurality of sequencers associated with respective subsets of the memory interfaces, and the algorithm controller issues each of the commands to the sequencers in parallel for application to the respective subsets of the memory interfaces (see Crouch, column 7 line 56 – column 8 line 3).

Referring to claim 5, Crouch teaches a set of command data interconnects to communicate the commands from the BIST controller to the plurality of sequencers and a set of acknowledgement interconnects to communicate acknowledge signals from the plurality of sequencers to the BIST controller to indicate the completion of the commands (see Crouch, column 8 lines 16-28).

Referring to claim 6, Crouch teaches that the sequencer controls an application speed of the memory operations to the memory interface in accordance with timing requirements of the memory module (see Crouch, column 8 lines 51-61).

Referring to claim 19, Crouch teaches that the commands conform to a generalized command protocol that substantially defines the test algorithm without regard to physical characteristics and timing requirements of the memory module (see Crouch, column 6 lines 7-14).

Referring to claim 22, Crouch teaches that the BIST controller, memory interface and sequencer are integrated within an electronic device (see Crouch, column 2 lines 6-9).

Referring to claim 23, Crouch teaches a system comprises: a plurality of memory modules (see Crouch, Figure 2); a built-in self-test (BIST) controller that stores an algorithm for testing the memory modules (see Crouch, Figure 2 "BIST Controller 210"); and a plurality of sequencers that are respectively coupled to different subsets of the memory modules, wherein each subset of the memory module is selected to include the memory modules having common clock domains, and each sequencer controls the application of the test algorithm to the respective subset of memory modules in accordance with the common clock domain of that subset of memory modules (see Crouch, column 7 line 56 – column 8 line 3).

Referring to claim 25, Crouch teaches a device comprising: first-level built-in self-test (BIST) means for issuing commands that define a BIST algorithm for a plurality of distributed memory modules having different timing requirements and physical

characteristics (see Crouch, Figure 2 "BIST Controller 210"); second-level BIST means for processing the commands to generate sequences of memory operations in accordance with the timing requirements of the memory modules (see Crouch, column 2 lines 6-9); and third-level BIST means for generating translated address and data signals from the memory operations based on the physical characteristics of the memory modules to apply the BIST algorithm to the distributed memory modules (see Crouch, Figure 2 "Memory 215").

Referring to claim 26, Crouch teaches algorithm storage means for storing the commands as one of a set of selectable memory test algorithms having associated commands (see Crouch, column 6 lines 10-18); and algorithm control means for retrieving the commands from the algorithm memory and issuing the commands associated with the selected memory test algorithm to the sequencer (see Crouch, column 6 lines 18-22).

Referring to claim 27, Crouch teaches a method comprising: issuing commands from a centralized BIST controller to a sequencer, wherein the commands define a memory test algorithm to be applied to a set of distributed memory modules without regard to physical characteristics or timing requirements of the memory modules (see Crouch, Figure 2 "BIST Controller 210"); processing the commands with the sequencer to generate one or more sequencers of memory operations in accordance with the timing requirements of the memory modules (see Crouch, column 2 lines 6-9); and

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applying the memory operations to the distributed memory modules to test the memory modules (see Crouch, Figure 2 "Memory 215").

Referring to claim 28, Crouch teaches translating address and data signals associated with the memory operations with memory interfaces coupled to each of the memory modules to generate translated address and data signals based on the physical characteristics of each of the memory modules, and wherein applying the memory operations comprises applying the translated address and data signals to test the memory modules (see Crouch, column 8 lines 4-28).

Referring to claim 29, Crouch teaches selecting the memory test algorithm from one of a plurality of memory test algorithms stored within an algorithm memory (see Crouch, column 6 lines 10-22).

### ***Claim Rejections - 35 USC § 103***

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 7-18, 20, 21, 24, 30 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Crouch et al. (U.S. Patent No. 5,995,731) (hereinafter Crouch) in view of Johnston et al. (U.S. Patent No. 6,272,588) (hereinafter Johnston).

Referring to claim 7, Crouch teaches that the sequencer comprises: a plurality of command controllers that implement the commands in accordance with a command protocol (see Crouch, Figure 2), but does not teach a command parser to parse each command to identify an operational code and a set of parameters based on the command protocol, wherein the command parser selectively invokes the command controllers based on the operational codes of the commands received from the BIST controller.

Johnston teaches a command parser to parse each command to identify an operational code and a set of parameters based on the command protocol (see Johnston, column 5 lines 4-9), wherein the command parser selectively invokes the command controllers based on the operational codes of the commands received from the BIST controller (see Johnston, column 5 lines 30-39).

It would have been obvious at the time the invention was made to one of ordinary skill in the art to modify Crouch to include the teachings of Johnston because parsing the data would have allowed the skilled artisan to separate and output the data (see Johnston, column 5 lines 7-9).

Referring to claim 8, Crouch teaches all the features of the claimed invention except that when invoked the command controllers issue the memory operations to the memory interface by sequencing through address ranges defined by the respective commands.

Johnston teaches that when invoked the command controllers issue the memory operations to the memory interface by sequencing through address ranges defined by the respective commands (see Johnston, column 5 lines 61-64).

It would have been obvious at the time the invention was made to one of ordinary skill in the art to modify Crouch to include the teachings of Johnston because issuing the memory operations in a sequence would have allowed the skilled artisan to detect as many failures as possible (see Johnston, column 5 lines 61-64).

Referring to claim 9, Crouch teaches all the features of the claimed invention except that the command controllers issue the memory operations by asserting signals to apply addresses and data to the memory interface based on the commands received from the BIST controller.

Johnston teaches that the command controllers issue the memory operations by asserting signals to apply addresses and data to the memory interface based on the commands received from the BIST controller (see Johnston, column 6 lines 6-14).

It would have been obvious at the time the invention was made to one of ordinary skill in the art to modify Crouch to include the teachings of Johnston because asserting signals to apply addresses and data to the memory would have allowed the skilled artisan to easily generate all necessary combinations of addresses and patterns (see Johnston, column 6 line 12-14).

Referring to claim 10, Crouch teaches all the features of the claimed invention except that the command controllers issue the memory operations by further asserting control signals to direct the memory interface to automatically store inverted data between at least one of neighboring rows, neighboring columns, and neighboring row-column matrices based on the physical characteristics of the memory module.

Johnston teaches that the command controllers issue the memory operations by further asserting control signals to direct the memory interface to automatically store inverted data between at least one of neighboring rows and neighboring columns based on the physical characteristics of the memory module (see Johnston, column 6 lines 1-14).

It would have been obvious at the time the invention was made to one or ordinary skill in the art to modify Crouch to include the teachings of Johnston because storing data would have allowed the skilled artisan to perform data retention testing (see Johnston, column 6 lines 32-36).

Referring to claim 11, Crouch teaches that based on the physical characteristics of the memory module the memory interface translates the addresses specified by the sequencer for the memory operations (see Crouch, column 8 lines 4-15).

Referring to claim 12, Crouch teaches all the features of the claimed invention except that the memory module includes memory cells arranged in rows and columns,

and the memory interface translates the addresses to fill the memory module in a row-wise or column-wise fashion as specified by the commands from the BIST controller.

Johnston teaches that the memory module includes memory cells arranged in rows and columns, and the memory interface translates the addresses to fill the memory module in a row-wise or column-wise fashion as specified by the commands from the BIST controller (see Johnston, column 6 lines 1-14).

It would have been obvious at the time the invention was made to one of ordinary skill in the art to modify Crouch to include the teachings of Johnston because having the BIST controller fill in the memory module would have allowed the skilled artisan to easily generate all necessary test combinations (see Johnston, column 6 lines 12-14).

Referring to claim 13, Crouch teaches all the features of the claimed invention except that the commands specify a bit pattern to be written to the memory module, and the memory interface translates the data specified by the sequencer based on the specified bit pattern and the physical characteristics of the memory module.

Johnston teaches that the commands specify a bit pattern to be written to the memory module, and the memory interface translates the data specified by the sequencer based on the specified bit pattern and the physical characteristics of the memory module (see Johnston, column 6 lines 6-14).

It would have been obvious at the time the invention was made to one of ordinary skill in the art to modify Crouch to include the teachings of Johnston because specifying

a bit pattern would have allowed the skilled artisan to easily generate all necessary test combinations (see Johnston, column 6 lines 12-14).

Referring to claim 14, Crouch teaches that the memory interface comprises a data generation unit that receives data signals from the sequencer and generates transformed data signals based on the data signals and the physical characteristics of the memory module (see Crouch, column 8 lines 4-28).

Referring to claim 15, Crouch teaches all the features of the claimed invention except that in response to a control signal received from the sequencer, the data generation unit automatically transforms the data to store inverted data within at least one of neighboring rows, neighboring columns, and neighboring row-column matrices of the memory module.

Johnston teaches that in response to a control signal received from the sequencer, the data generation unit automatically transforms the data to store inverted data within at least one of neighboring rows and neighboring columns of the memory module (see Johnston, column 6 lines 1-14).

It would have been obvious at the time the invention was made to one of ordinary skill in the art to modify Crouch to include the teachings of Johnston because storing data would have allowed the skilled artisan to perform data retention testing (see Johnston, column 6 lines 32-36).

Referring to claim 16, Crouch teaches all the features of the claimed invention except that he memory interface comprises an address generation unit that receives address signals from the sequencer and generates transformed address signals based on an arrangement of rows and columns of the memory module.

Johnston teaches that he memory interface comprises an address generation unit that receives address signals from the sequencer and generates transformed address signals based on an arrangement of rows and columns of the memory module (see Johnston, column 5 line 61 – column 6 line 14).

It would have been obvious at the time the invention was made to one of ordinary skill in the art to modify Crouch to include the teachings of Johnston because generating address signals would have allowed the skilled artisan to generate test reads and test writes (see Johnston, column 6 lines 1-3).

Referring to claim 17, Crouch teaches all the features of the claimed invention except that the memory interface comprises a comparator to compare data read from the memory module to data previously written to the memory module and set a state of a failure signal based on the comparison.

Johnston teaches that the memory interface comprises a comparator to compare data read from the memory module to data previously written to the memory module and set a state of a failure signal based on the comparison (see Johnston, column 4 lines 4-9).

It would have been obvious at the time the invention was made to one of ordinary skill in the art to modify Crouch to include the teachings of Johnston because comparing the data would have allowed the skilled artisan to test the retention time (see Johnston, column 7 lines 12-18).

Referring to claim 18, Crouch teaches all the features of the claimed invention except that the physical characteristics include at least one of a number of rows, a number of columns, and a number of row-column matrices of the memory module.

Johnston teaches that the physical characteristics include at least one of a number of rows and a number of columns of the memory module (see Johnston, column 3 lines 21-31).

It would have been obvious at the time the invention was made to one of ordinary skill in the art to modify Crouch to include the teachings of Johnston because accounting for the rows or columns would have allowed the skilled artisan to easily incorporate the BIST into existing architecture (see Johnston, column 3 lines 13-19).

Referring to claim 20, Crouch teaches all the features of the claimed invention except that the command protocol defines a command syntax having a set of supported commands, and each command includes an operand and a set of parameters.

Johnston teaches that the command protocol defines a command syntax having a set of supported commands, and each command includes an operand and a set of parameters (see Johnston, column 4 lines 40-53).

It would have been obvious at the time the invention was made to one of ordinary skill in the art to modify Crouch to include the teachings of Johnston because having a command including an operand and a set of parameters would have allowed the skilled artisan to ensure that data is not lost over time by normal current leakage (see Johnston, column 4 lines 53-58).

Referring to claim 21, Crouch teaches all the features of the claimed invention except that at least one of the commands includes fields to specify an address range, one or more memory operations to apply over the address range, and a bit pattern for application to the memory module of the address range.

Johnston teaches that at least one of the commands includes fields to specify an address range, one or more memory operations to apply over the address range, and a bit pattern for application to the memory module of the address range (see Johnston, column 6 lines 6-14).

It would have been obvious at the time the invention was made to one of ordinary skill in the art to modify Crouch to include the teachings of Johnston because specifying a bit pattern would have allowed the skilled artisan to easily generate all necessary test combinations (see Johnston, column 6 lines 12-14).

Referring to claim 24, Crouch teaches all features of the claimed invention except a plurality of memory interfaces that are respectively coupled to the memory modules, wherein each of the memory interfaces receive address and data signals generated by

the sequencer based on the algorithm and translates the address and data signals in accordance with an arrangement of rows and columns of the respective memory module.

Johnston teaches a plurality of memory interfaces that are respectively coupled to the memory modules, wherein each of the memory interfaces receive address and data signals generated by the sequencer based on the algorithm and translates the address and data signals in accordance with an arrangement of rows and columns of the respective memory module (see Johnston, column 5 line 61 – column 6 line 14).

It would have been obvious at the time the invention was made to one of ordinary skill in the art to modify Crouch to include the teachings of Johnston because generating address signals would have allowed the skilled artisan to generate test reads and test writes (see Johnston, column 6 lines 1-3).

Referring to claim 30, Crouch teaches all the features of the claimed invention except translating address and data signals with memory interfaces based on at least one of a number of rows of the respective memory module, a number of columns of the respective memory module, and a number of row-column matrices of the respective memory module.

Johnston teaches translating address and data signals with memory interfaces based on at least one of a number of rows of the respective memory module and a number of columns of the respective memory module of the respective memory module (see Johnston, column 6 lines 1-14).

It would have been obvious at the time the invention was made to one of ordinary skill in the art to modify Crouch to include the teachings of Johnston because accounting for the rows or columns would have allowed the skilled artisan to easily incorporate the BIST into existing architecture (see Johnston, column 3 lines 13-19).

Referring to claim 31, Crouch teaches all the features of the claimed invention except issuing commands in accordance with a command protocol that defines a set of supported commands having operands and a set of parameters that define the memory operations to be generated by the sequencer.

Johnston teaches issuing commands in accordance with a command protocol that defines a set of supported commands having operands and a set of parameters that define the memory operations to be generated by the sequencer (see Johnston, column 4 lines 40-53).

It would have been obvious at the time the invention was made to one of ordinary skill in the art to modify Crouch to include the teachings of Johnston because having a command including an operand and a set of parameters would have allowed the skilled artisan to ensure that data is not lost over time by normal current leakage (see Johnston, column 4 lines 53-58).

### ***Conclusion***

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- (a) Adams et al. teach a system initialization of microcode-based memory built-in self-test.
- (b) Geiger et al. teach at-speed computer model testing methods.
- (c) Slobodnik teaches a method and apparatus for memory self testing.
- (d) Hill et al. teach a restartable logic BIST controller.
- (e) Rajska et al. teach a method and apparatus for selectively compacting test responses.
- (f) Rieken teaches an apparatus and method for implementing a wireless system-on-a-chip with a reprogrammable tester, debugger, and bus monitor.
- (g) Jun teaches a programmable built-in self-test system for semiconductor memory device.
- (h) Aipperspach et al. teach stability test for silicon on insulator SRAM memory cells utilizing bitline precharge stress operations to stress memory cells under test.
- (i) Resnick teaches a method and apparatus for partial-scan built-in self-test logic.
- (j) Rajsuman et al. teach a method and structure for testing embedded memories.

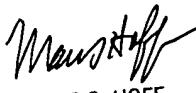
6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mary Kate B. Baran whose telephone number is (571)

272-2211. The examiner can normally be reached on Monday - Friday from 9:00 am to 6:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Marc S. Hoff can be reached on (571) 272-2216. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

15 April 2005



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